

Υποθετικός Πολυνηματισμός

Τα προβλήματα του παράλληλου προγραμματισμού

- Εντοπισμός παραλληλισμού
 - χειροκίνητα (επισκόπηση)
 - αυτόματα (compiler)
- Έκφραση παραλληλισμού
 - low-level (π.χ. Pthreads, MPI)
 - high-level (π.χ. OpenMP, Cilk, Intel TBB, Galois, UPC κ.λπ.)
- Απεικόνιση
 - scheduling, creation, termination, etc.
 - operating system, runtime system
- Συγχρονισμός
 - εύκολος όπως ο coarse-grain
 - αποδοτικός όπως ο fine-grain
 - deadlock-free
 - composable
- Απαιτήσεις
 - κλιμακωσιμότητα
 - ευκολία προγραμματισμού
 - υψηλή παραγωγικότητα
 - ορθότητα
 - architectural awareness

Parallelizing Compilers

- Στοχεύουν σε «κανονικές» εφαρμογές
 - for loops, arrays
 - (παραδοσιακά, HPC scientific codes...)
- Συνήθως, 2 περάσματα:
 - Είναι ένα loop «ασφαλές» για παραλληλοποίηση;
 - στατική ανάλυση (dependence, alias)
 - «Αξίζει» να παραλληλοποιηθεί;
 - cost model, profiling
 - Παραδείγματα: Intel CC, SUIF-1, Polaris, PGI, Open64
- Τι γίνεται με τις «ακανόνιστες» εφαρμογές;
 - ασαφείς/μη-σταθερές εξαρτήσεις (π.χ. input dependent)
 - «περίπλοκες» δομές

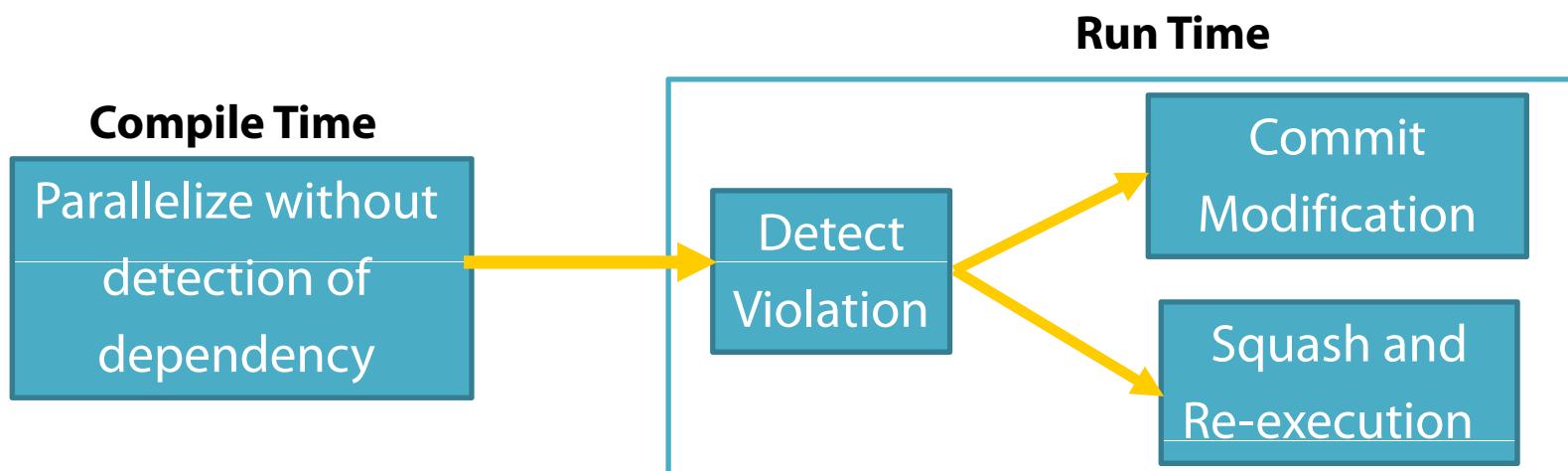
Ενδεικτική κατηγοριοποίηση

Χαρακτηριστικά κώδικα	Παράδειγμα	Πεδίο εφαρμογής
Arrays with direct addressing	<pre>for(i = 1; i<n; i++) { A[i] = B[i]*C[i]; }</pre>	<ul style="list-style-type: none">scientific codesmedia applications
Arrays with indirect addressing	<pre>for(i = 1; i<n; i++) { z = A[K[i]]; A[L[i]] = z + C[i]; }</pre>	<ul style="list-style-type: none">circuit simulationsstructural mechanics modelingmolecular dynamics simulationfluid flows
Recursive Data Structures (RDS): <ul style="list-style-type: none">treeslistsgraphssetshash-tables...	<pre>while(ptr=ptr->next) { ProcessElement(ptr->val); }</pre>	<ul style="list-style-type: none">graph algorithms (shortest paths, minimum spanning trees, max flows)simulations (N-body, graphics)meshes (refinement, triangulation)dynamic programmingdata mining...

Υποθετικός Πολυνηματισμός

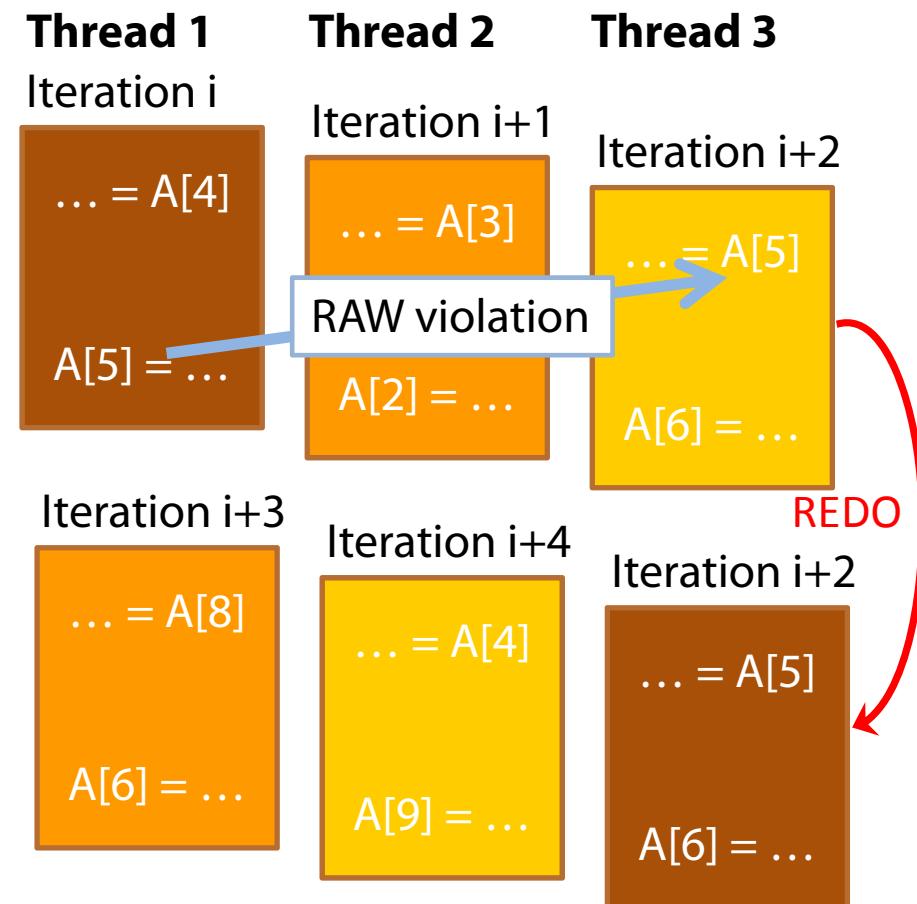
Speculative Multithreading or Thread-Level Speculation

- επιτρέπει τη δημιουργία και εκτέλεση παράλληλων νημάτων παρά τις πιθανές εξαρτήσεις δεδομένων
- ελπίζουμε στην μη-ύπαρξη εξαρτήσεων
 - «αισιόδοξος» παραλληλισμός



Παράδειγμα

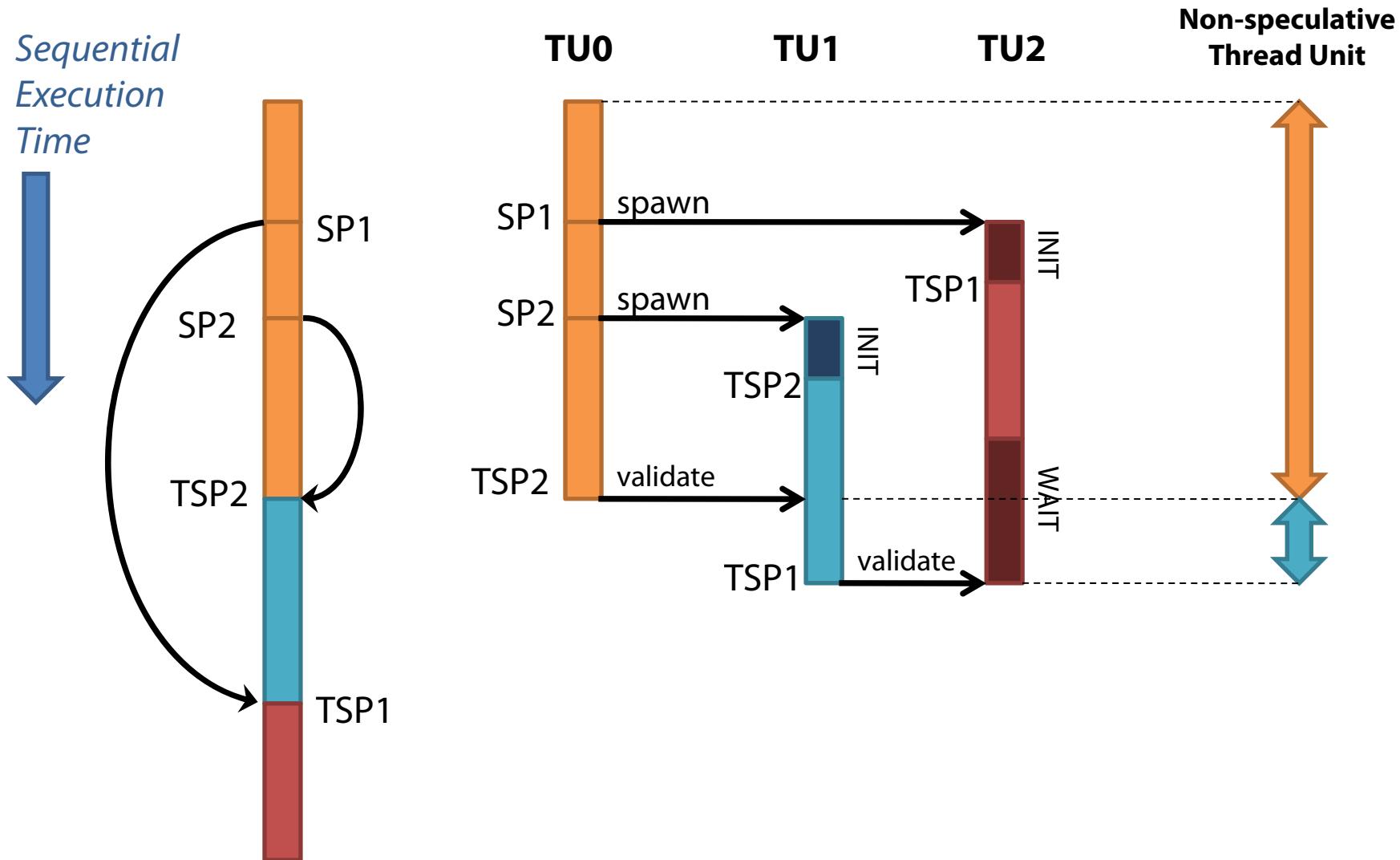
```
for(i =0; i <n; i++) {  
    ... = A[B[i]];  
    ...  
    A[C[i]] = ...  
}
```



Γενικό Μοντέλο

- 1 main (non-speculative) thread
 - γηραιότερο
 - το μόνο που επιτρέπεται να κάνει commit
- $N \geq 0$ speculative threads
- σχέσεις predecessor-successor ανάμεσα στα threads
 - sequential semantics
- οποιοδήποτε thread μπορεί να κάνει spawn κάποιο άλλο (speculative) thread

Γενικό Μοντέλο

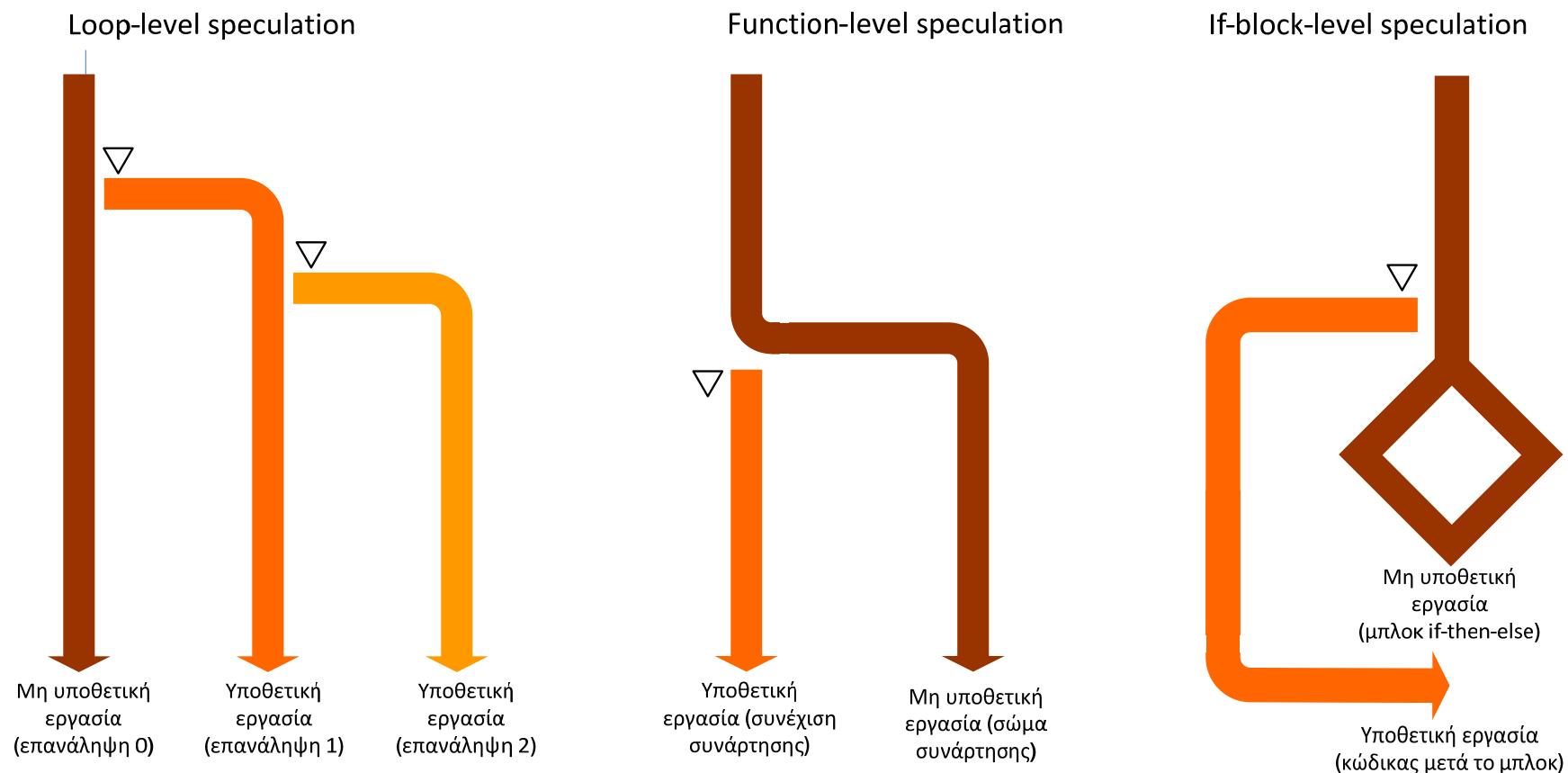


SP: spawning point

TSP: thread start point

Προγραμματιστικές Δομές

- Ξεκινάμε από το σειριακό πρόγραμμα και εξάγουμε «**ordered**» νήματα (ή εργασίες)



Υποθετικός Πολυνηματισμός

Το HW/SW (runtime system) παρέχει υποστήριξη για:

- **checkpointing** των καταχωρητών στην αρχή της εκτέλεσης μιας εργασίας
- **buffering** της υποθετικής κατάστασης που δημιουργείται
 - π.χ. write-buffer, cache
- **παρακολούθηση** των λειτουργιών μνήμης των εργασιών
 - παραβίαση εξαρτήσεων: **αναίρεση** των επιδράσεων της (πιο) υποθετικής εργασίας και **επανεκκίνηση**
 - π.χ. απόρριψη write-buffer, restore registers
 - μη παραβίαση εξαρτήσεων: **commit** αποτελεσμάτων των εργασιών
 - στη σειρά προγράμματος!

Παράδειγμα Ανίχνευσης Παραβιάσεων

- Επέκταση cache με
 - timestamp («epoch number»): δείχνει τη σειρά στο σειριακό πρόγραμμα
 - violation flag
- Επέκταση cache line με ειδικά bits
 - SL: κάποιο speculative load έχει προσπελάσει την cache line
 - SM: η γραμμή έχει τροποποιηθεί υποθετικά
- Σε κάθε write-invalidation, μια εργασία μαρκάρεται για ακύρωση αν:
 - η γραμμή είναι παρούσα στην cache της
 - το SL bit της είναι set
 - το «epoch number» του invalidator υποδεικνύει προγενέστερο νήμα στη σειρά προγράμματος

Παράδειγμα Ανίχνευσης Παραβιάσεων

Processor 1
Epoch 5

$p = q = \&x$

...

②`STORE *q = 2;`

...

L1 Cache

Epoch # = 5
Violation? = FALSE

Processor 2

Epoch 6

`become_speculative()`

①`LOAD a = *p;`

...

③`attempt_commit();`

...

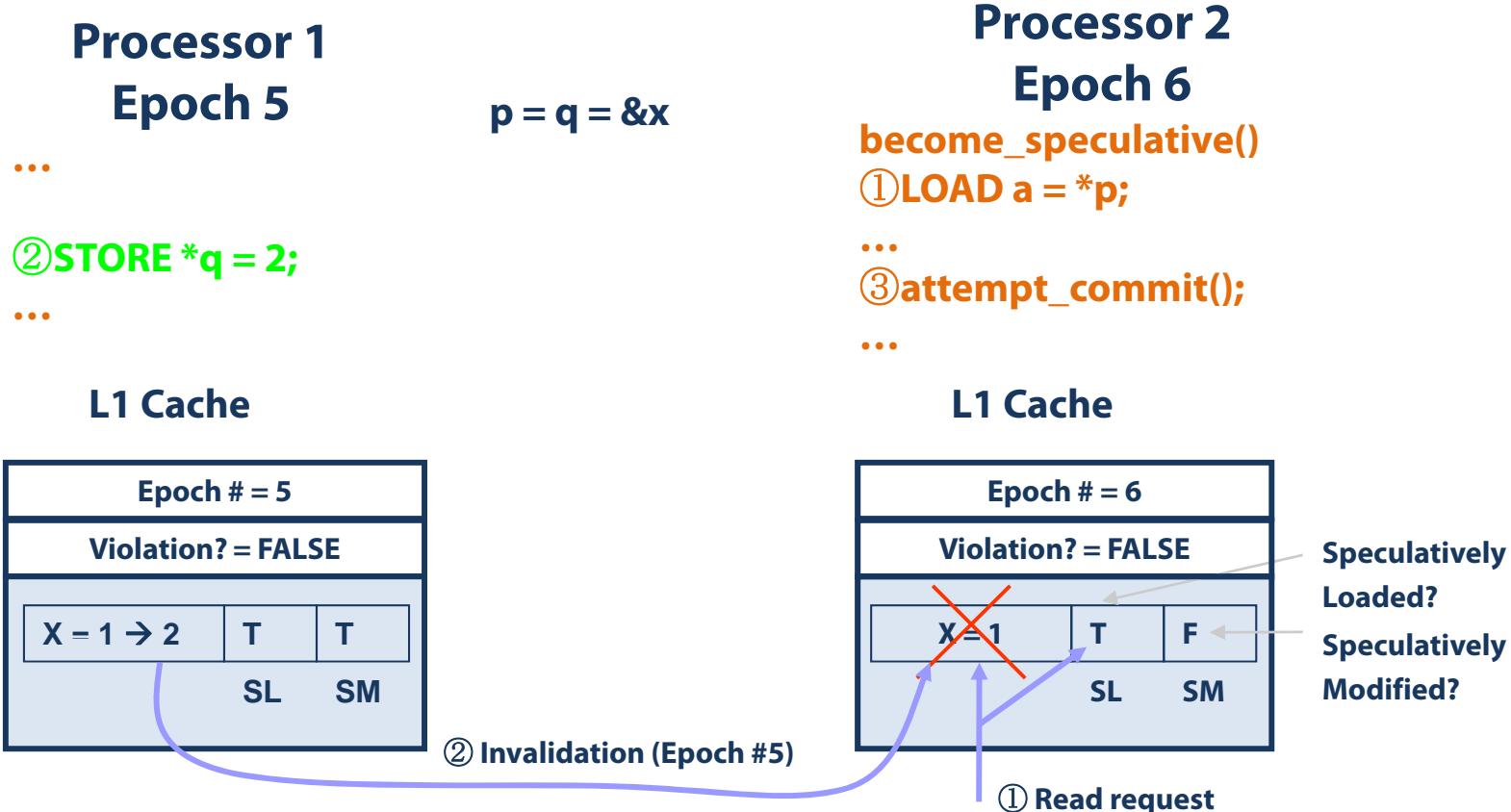
L1 Cache

Epoch # = 6
Violation? = FALSE
X = 1 T F SL SM

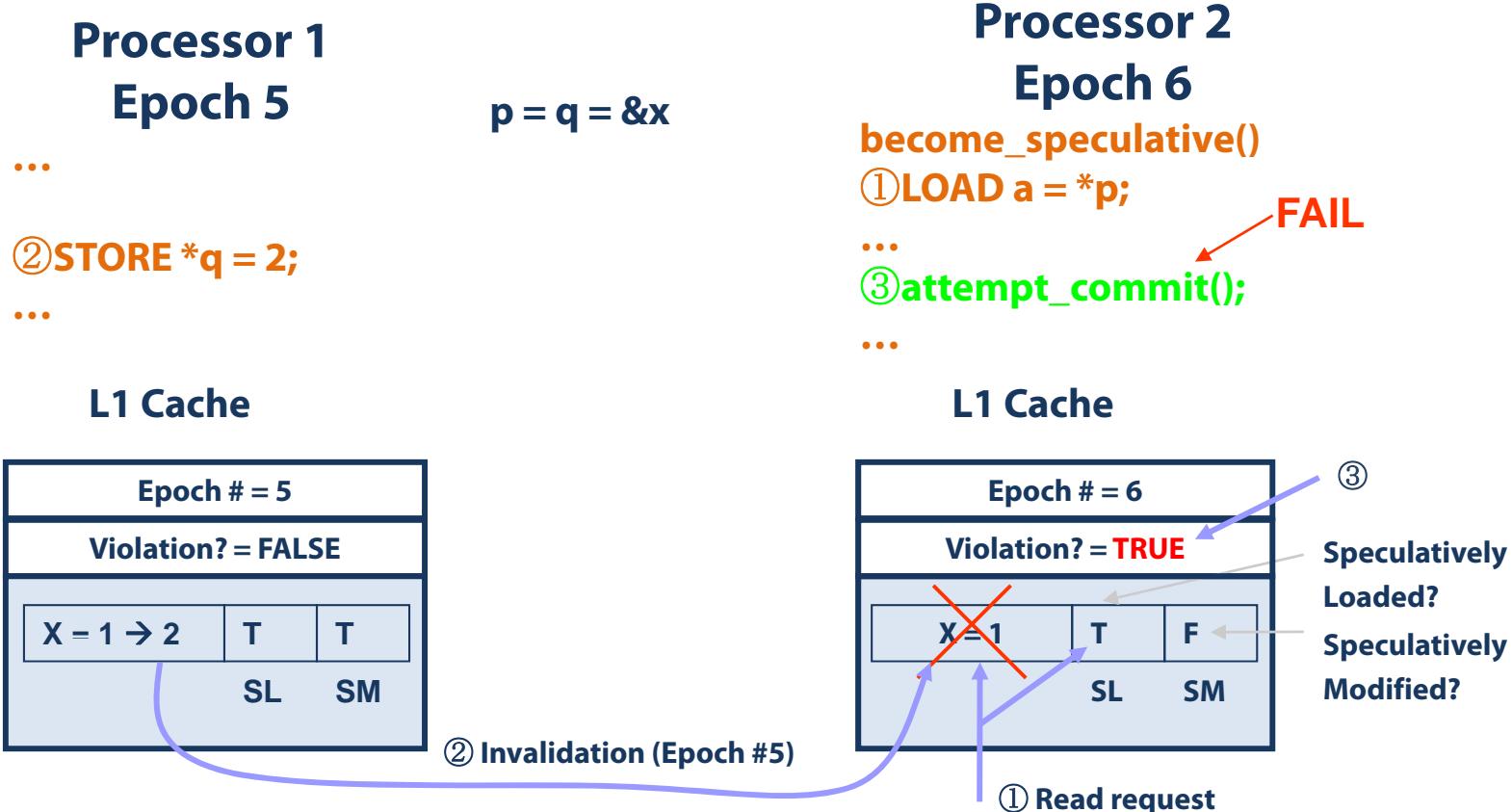
① `Read request`

Speculatively
Loaded?
Speculatively
Modified?

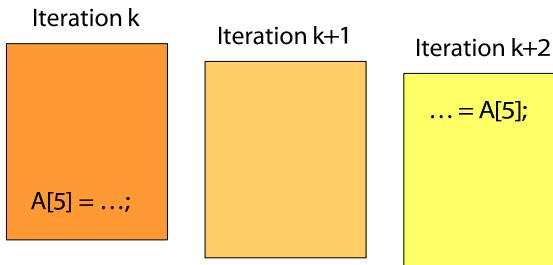
Παράδειγμα Ανίχνευσης Παραβιάσεων



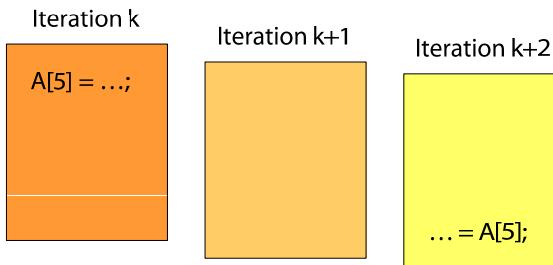
Παράδειγμα Ανίχνευσης Παραβιάσεων



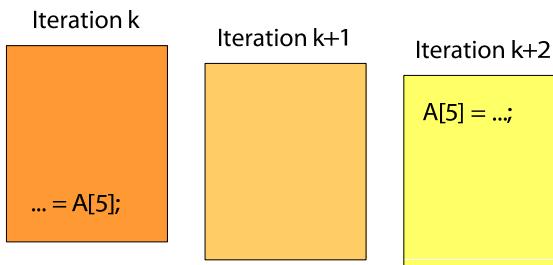
Τι εξαρτήσεις μας νοιάζουν τελικά;



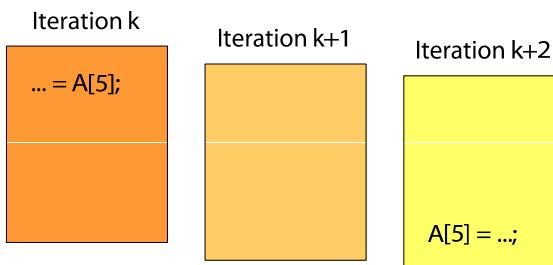
RAW dependence violated:
violates sequential semantics (k's store
should have preceded k+2's load in
program order)



RAW dependence respected:
no problem (theoretically), but requires
data forwarding mechanism



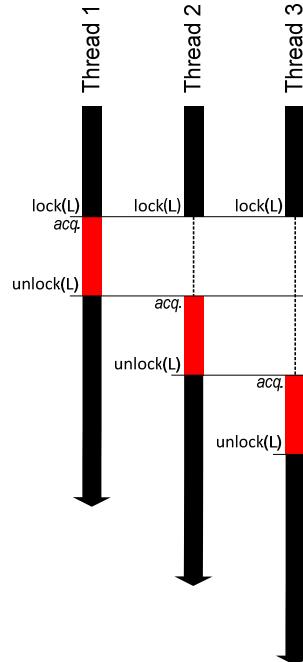
WAR dependence violated:
no problem if speculative writes are
being buffered



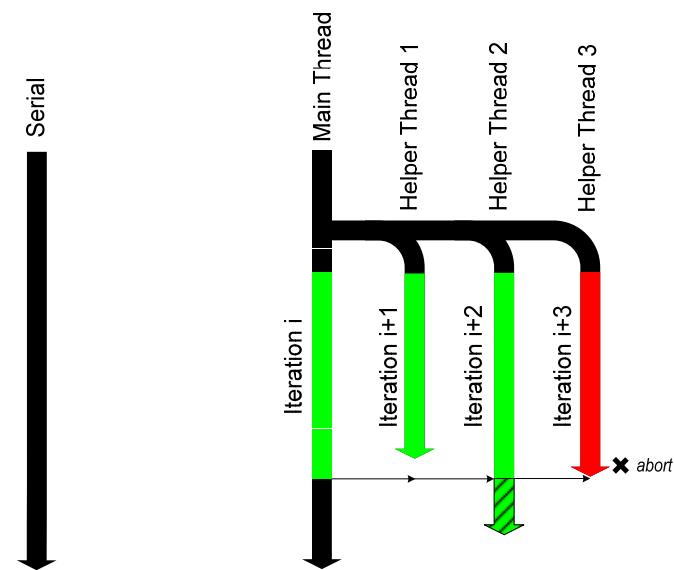
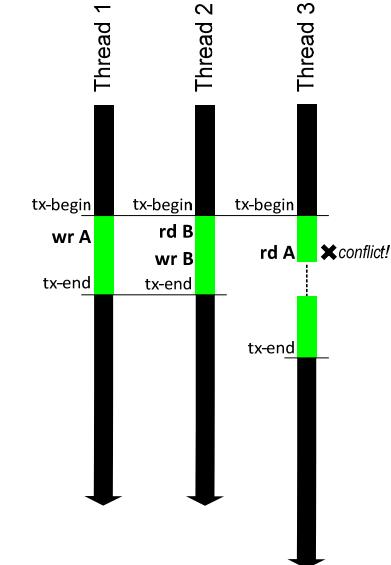
WAR dependence respected:
no problem

TM vs TLS

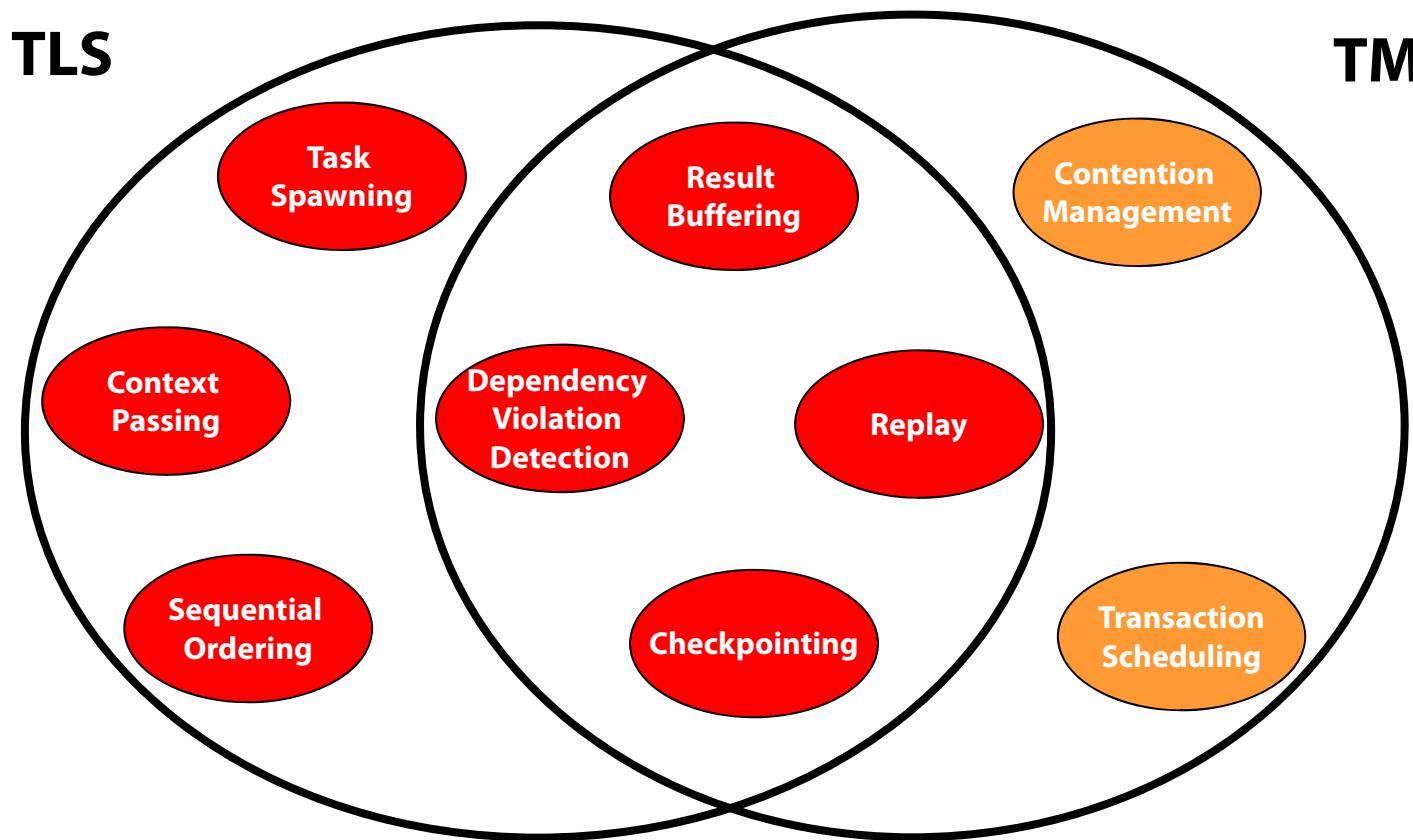
- αισιόδοξος συγχρονισμός



- αισιόδοξος παραλληλισμός



TM vs TLS



TLS and TM share multiple hardware components

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