Computer History & Computer Characteristics

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Integrated Circuit

In 1959 both parties applied for patents. Jack Kilby and Texas Instruments received U.S. patent #3,138,743 for miniaturized electronic circuits. Robert Noyce and the Fairchild Semiconductor Corporation received U.S. patent #2,981,877 for a silicon based integrated circuit. The two companies wisely decided to cross license their technologies after several years of legal battles, creating a global market now worth about $1 trillion a year.

"What we didn't realize then was that the integrated circuit would reduce the cost of electronic functions by a factor of a million to one, nothing had ever done that for anything before" - Jack Kilby
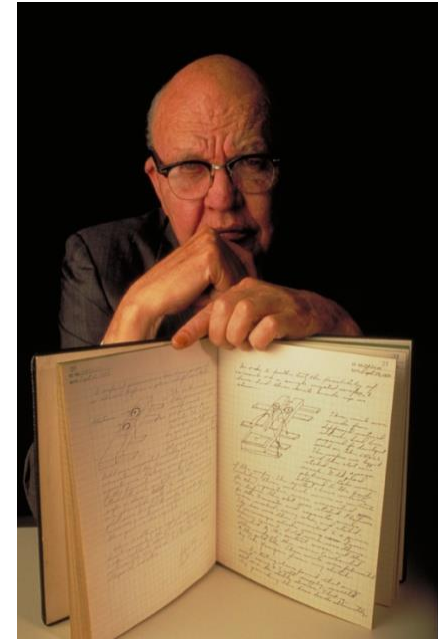
The USA patent for the first integrated circuit
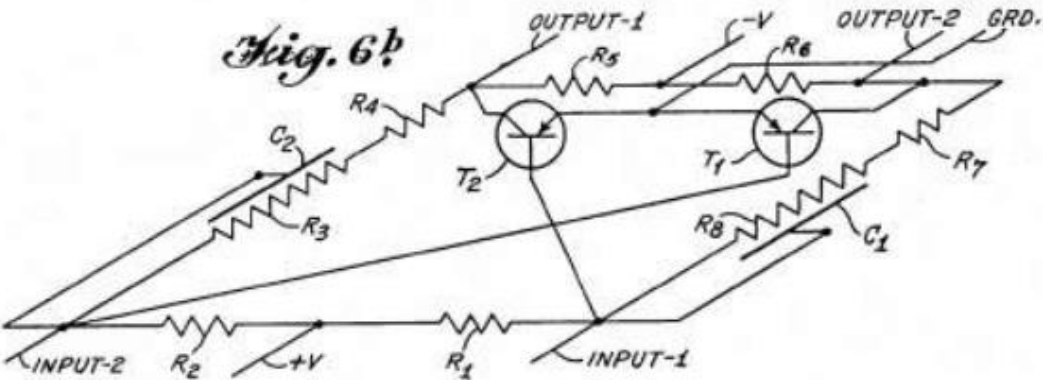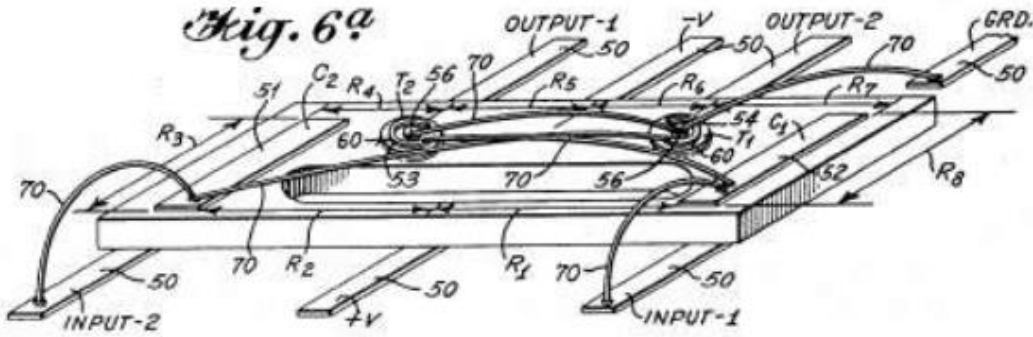

June 23, 1964   J. S. KILBY   3,138,743

MINIATURIZED ELECTRONIC CIRCUITS

Filed Feb. 6, 1959   4 Sheets—Sheet 2

Computing at Manchester after WWII
Mark I

The University of Manchester made a considerable contribution to the development of computing. They produced the first stored program computer, the first floating point machine, the first transistor computer and the first computer to use virtual memory.
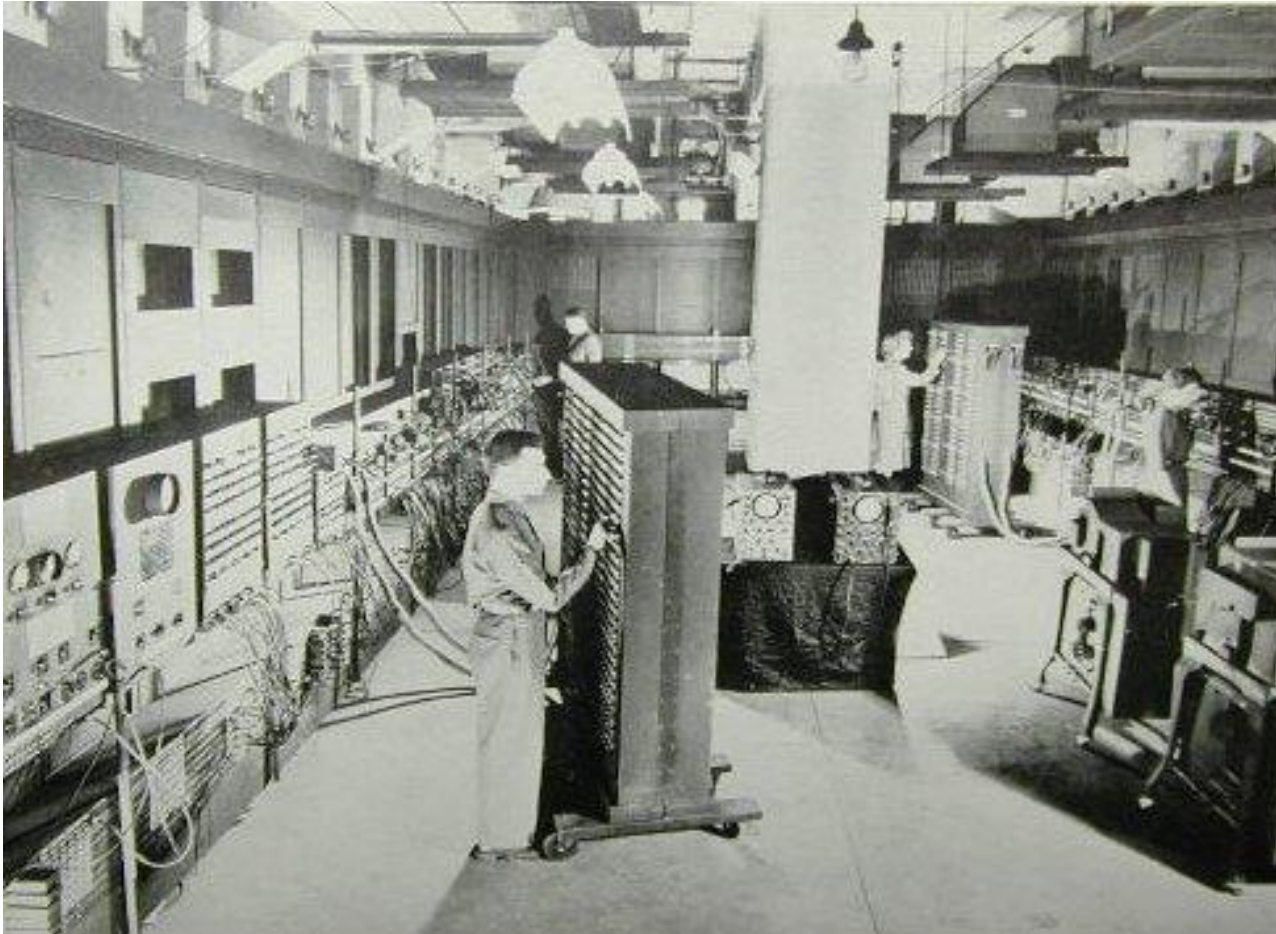

Right Images of Mark 1 the computer built at Manchester University after WWII
Above Kilburn and Williams at the Manchester Mark 1 Console
http://www.computer50.org/kgill/index.html
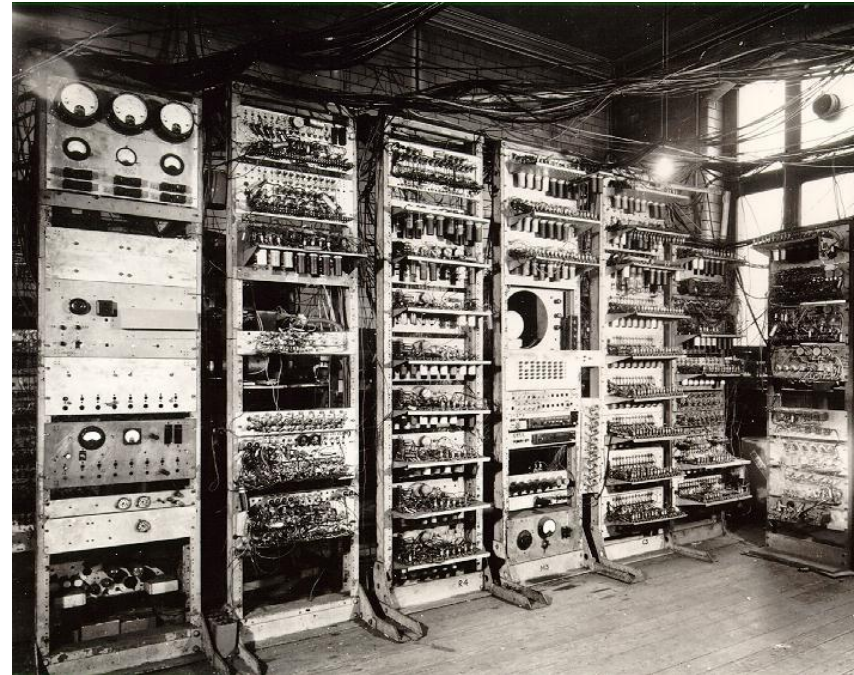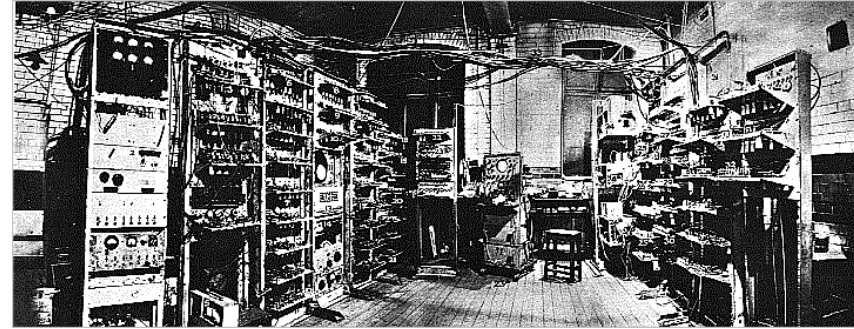
ENIAC (Electronic Numerical Integrator and Computer)
## U.S. Army Computer @ University of Pennsylvania

o ENIAC contained approximately 18,000 vacuum tubes, 70,000 resistors, 10,000 capacitors, and 6,000 switches.

o It was 100 feet long, 10 feet high, and 3 deep. It consumed 140 kilowatts of power.
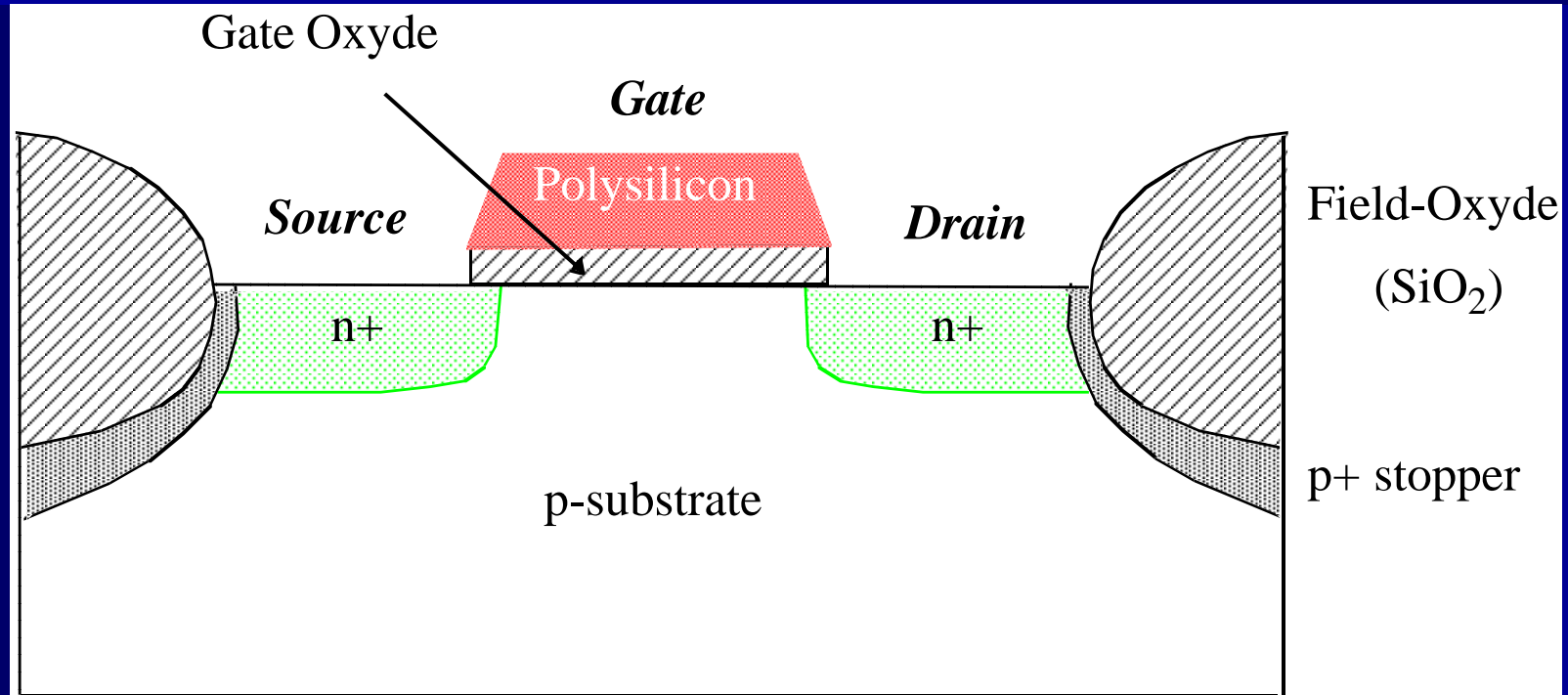
The Transistor

John <u>Bardeen</u>, Walter <u>Brattain</u> and William <u>Shockley</u> discovered the transistor effect and developed the first device in December 1947, while the three were members of the technical staff at Bell Laboratories in Murray Hill, NJ. They were awarded the Nobel Prize in physics in 1956.

Developed as a replacement for bulky and inefficient vacuum tubes and mechanical relays, the transistor later revolutionized the entire electronics world.
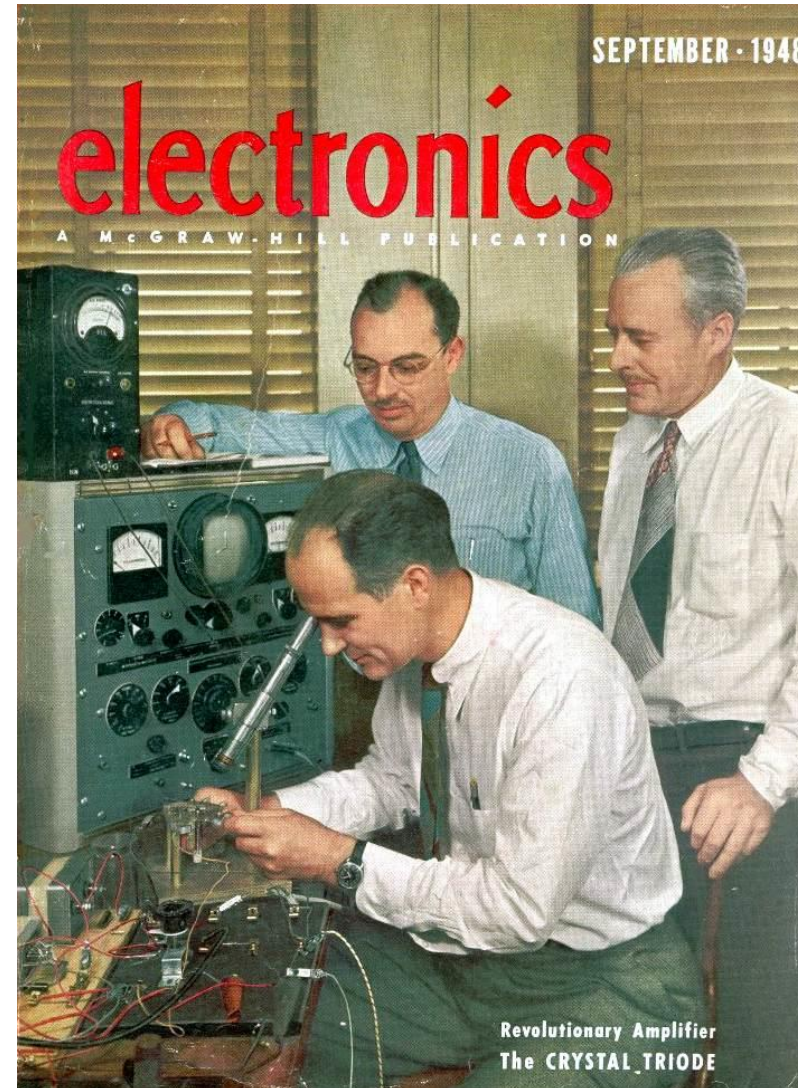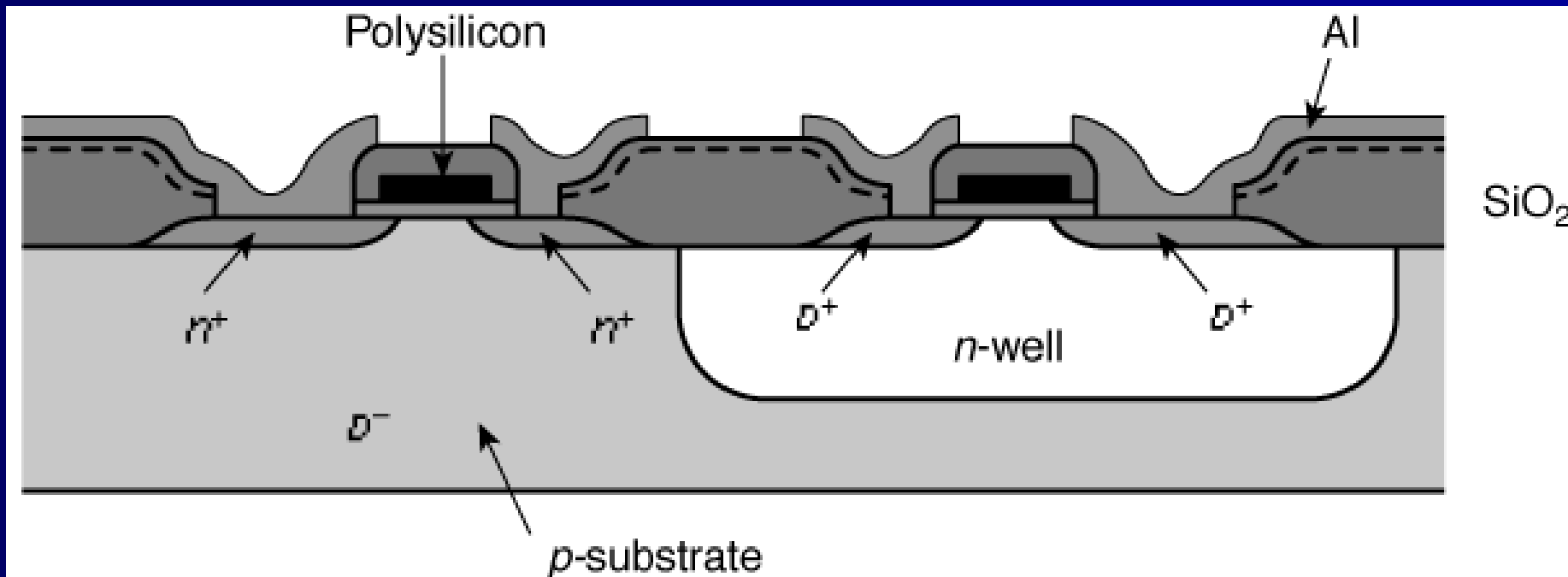
The MOS Transistor

CROSS-SECTION of NMOS Transistor

Cross-Section of CMOS Technology

Intel

1950's: Shockley leaves Bell Labs to establish Shockley Labs in California. Some of the best young electronic engineers and solid-state physicists come to work with him. These include Robert Noyce and Gordon Moore.

1969: <u>Intel</u> was a tiny start-up company in Santa Clara, headed by Noyce and <u>Moore</u>.

1970: <u>Busicom</u> placed an order with Intel for custom calculator chips. Intel had no experience of custom-chip design and sets outs to design a <u>general-purpose solution</u>.

1971: Intel have problems translating architectures into working chip designs – the project runs late.

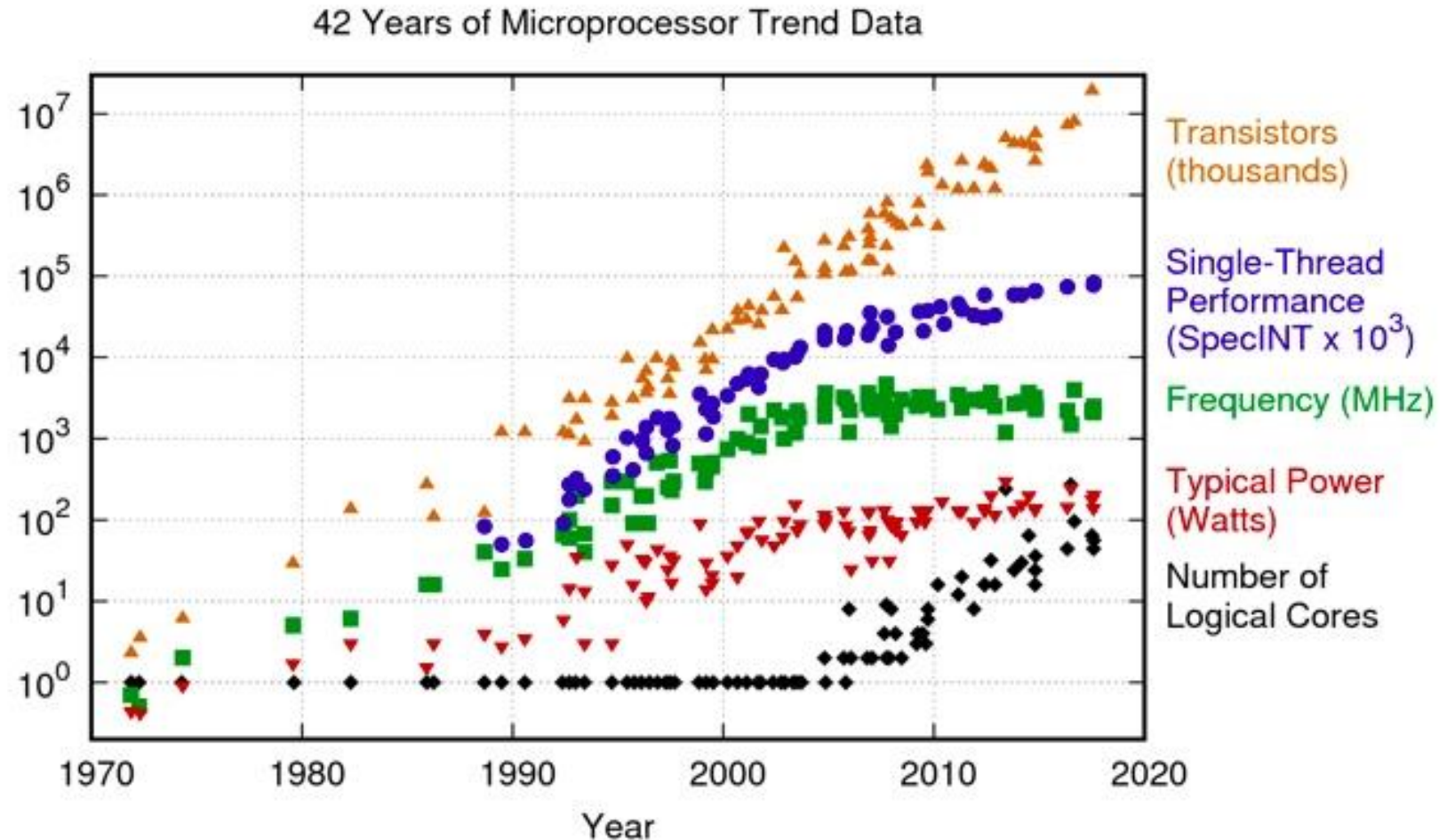<u>Faggin</u> joins Intel and solves the problems in weeks.

The result is the <u>Intel 4000 family</u> (later renamed MCS-4, Microcomputer System 4-bit), comprising the 4001 (2k ROM), the 4002 (320-bit RAM), the 4003 (10-bit I/O shift-register) and the <u>4004</u>, a 4-bit CPU.

Moore's Law

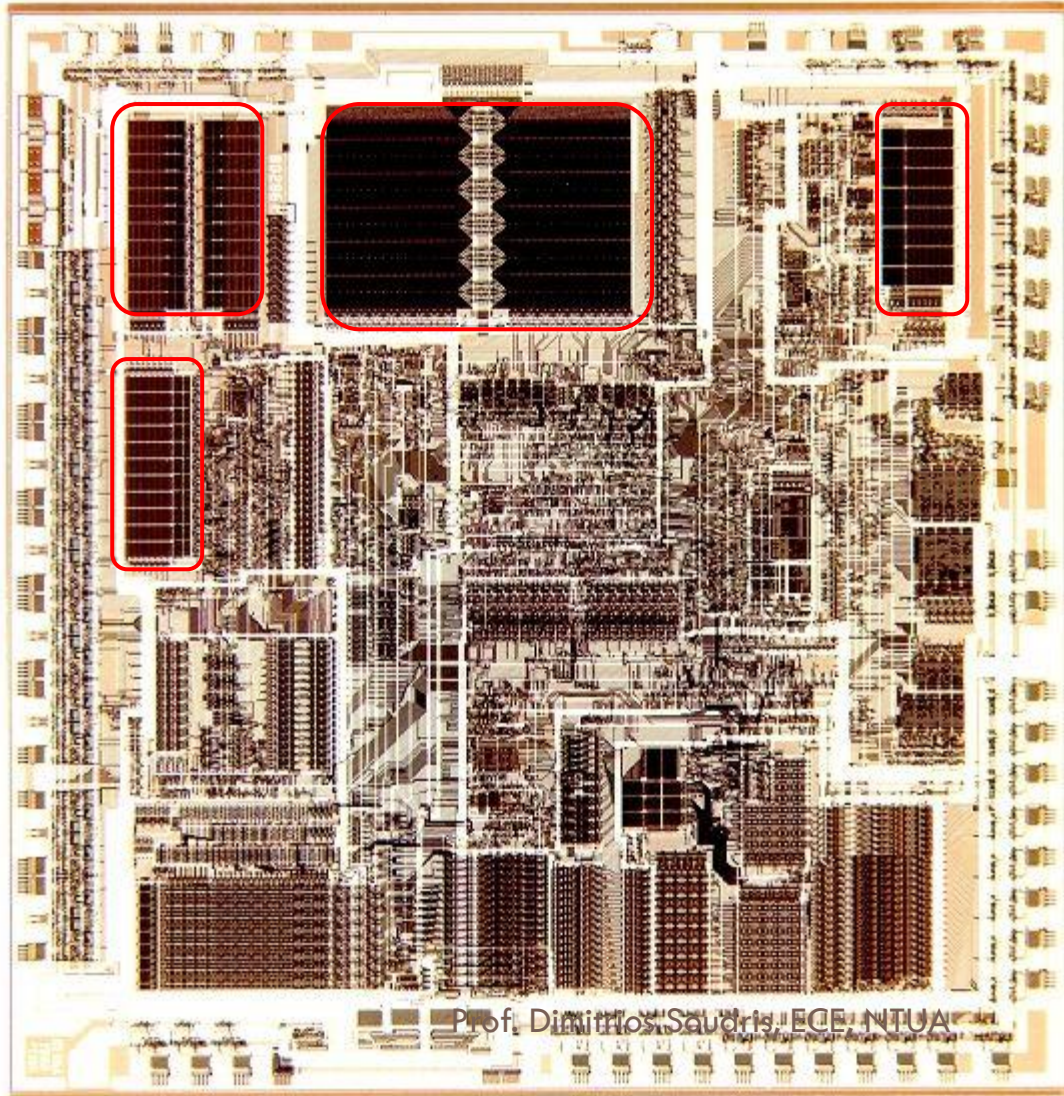Dr. Gordon E. Moore co-founded Intel in 1968.

His observation that number of transistors doubled every two years became known as "Moore's Law"

42 Years of Microprocessor Trend Data

Transistors (thousands)
Single-Thread Performance (SpecINT x 10^3)
Frequency (MHz)
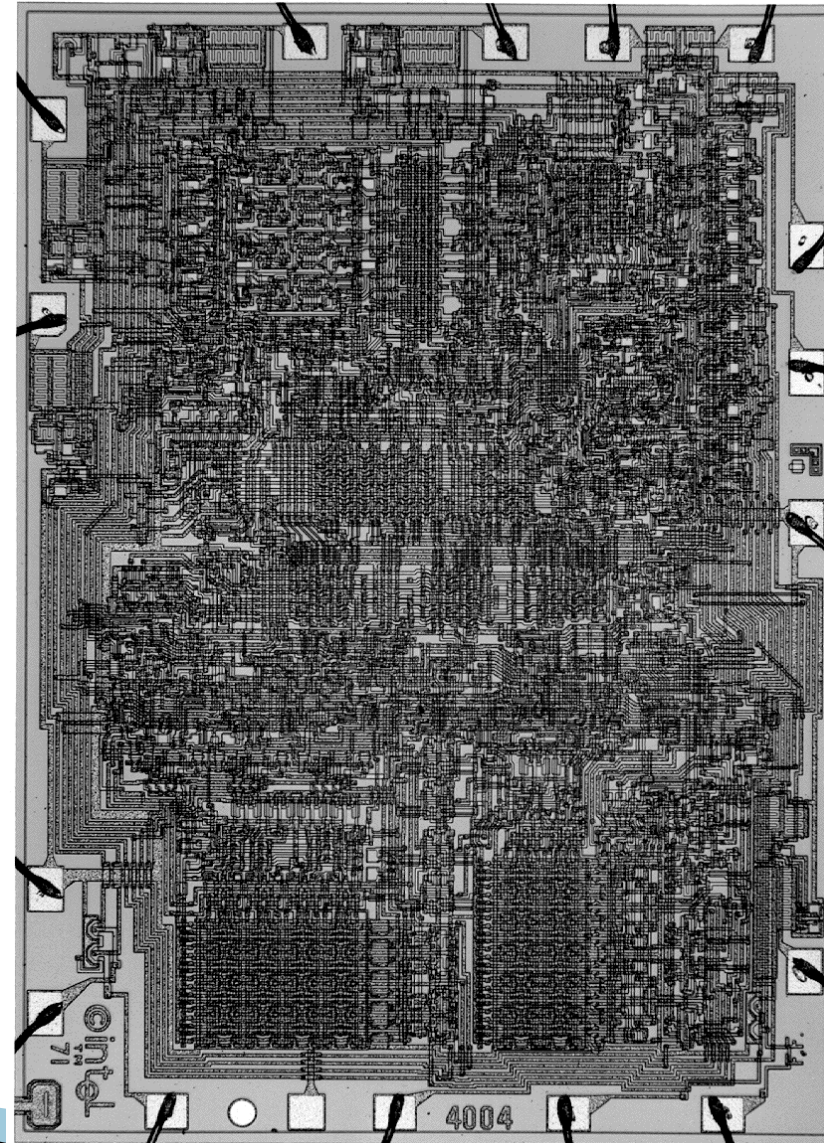Typical Power (Watts)
Number of Logical Cores

Original data up to the year 2010 collected and plotted by M. Horowitz, F. Labonte, O. Shacham, K. Olukotun, L. Hammond, and C. Batten
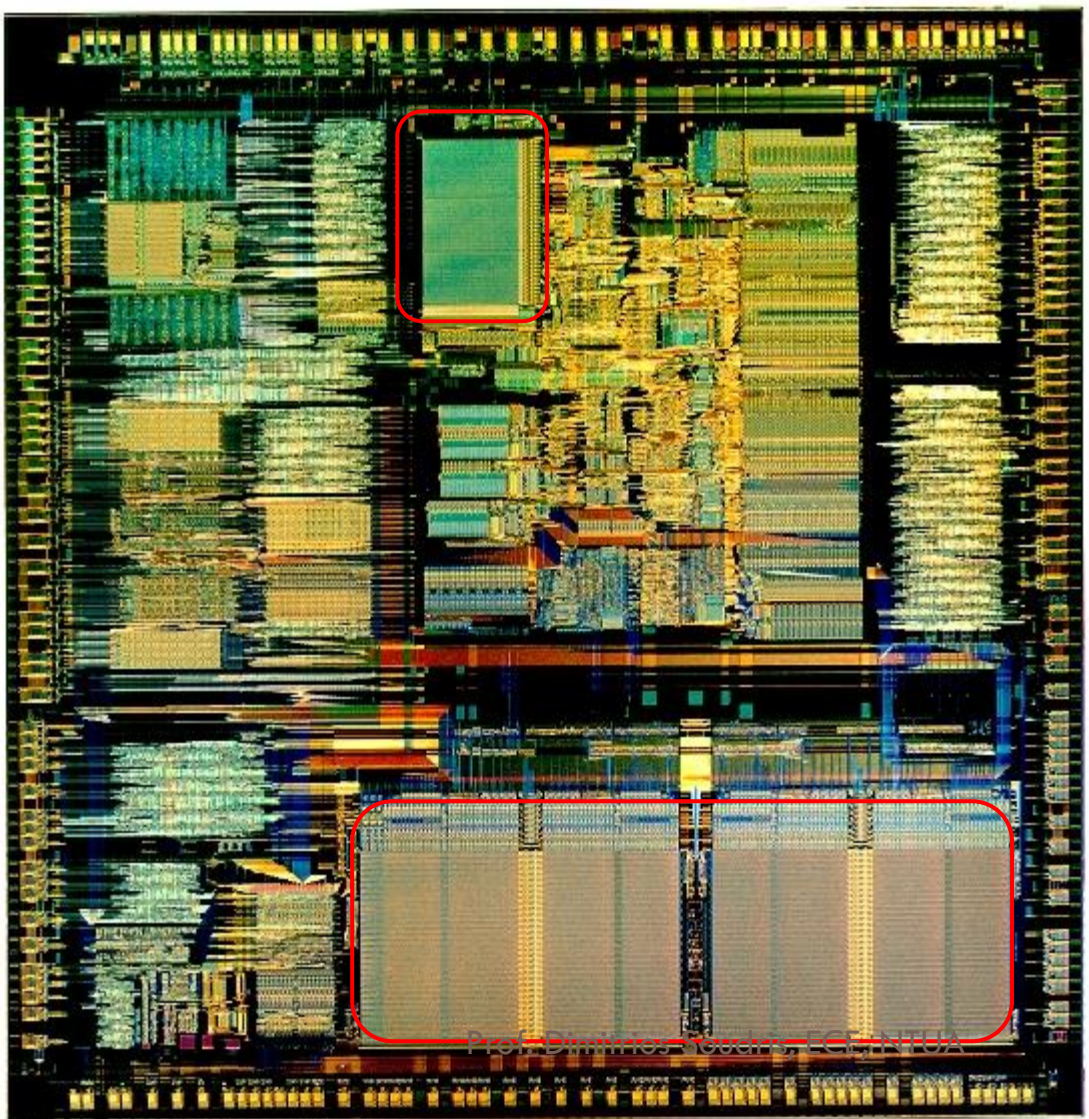New plot and data collected for 2010-2017 by K. Rupp

https://www.karlrupp.net/2018/02/42-years-of-microprocessor-trend-data/

Intel Microprocessor – 286
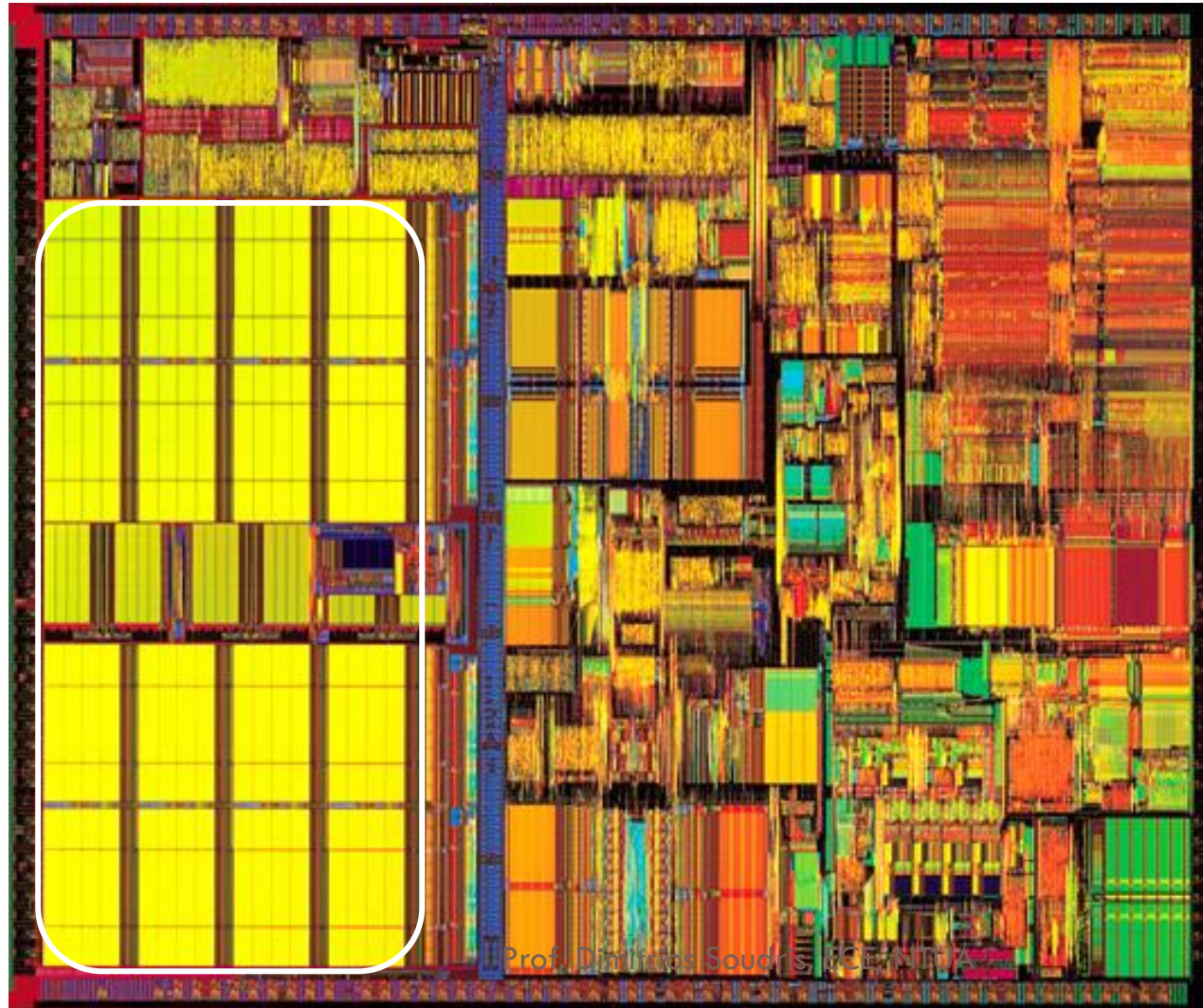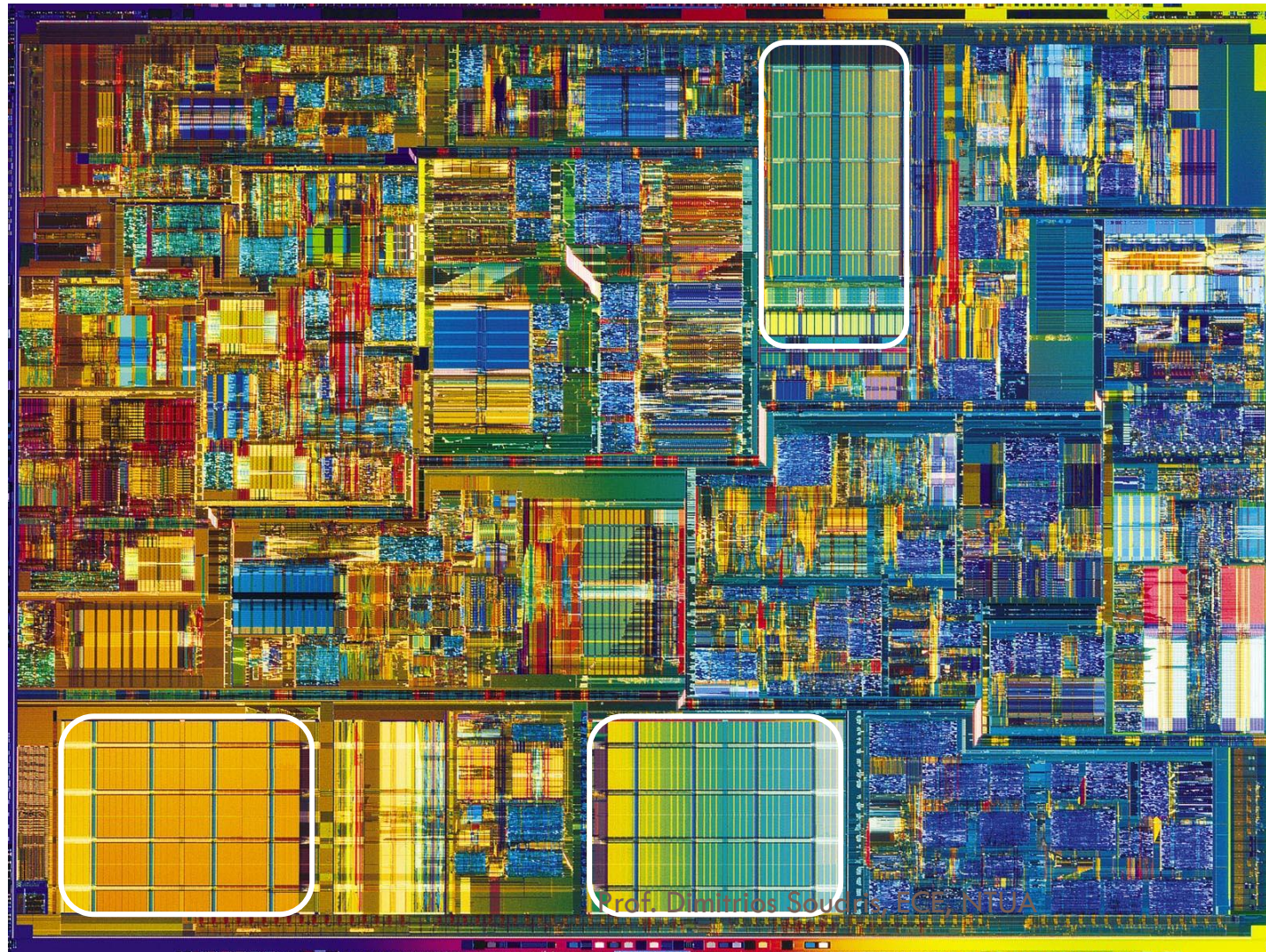
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Intel 4004 Micro-Processor

Intel Microprocessor – 386

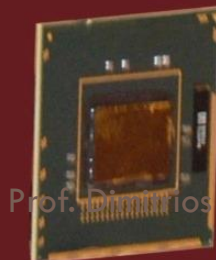# Intel Microprocessor – Pentium III
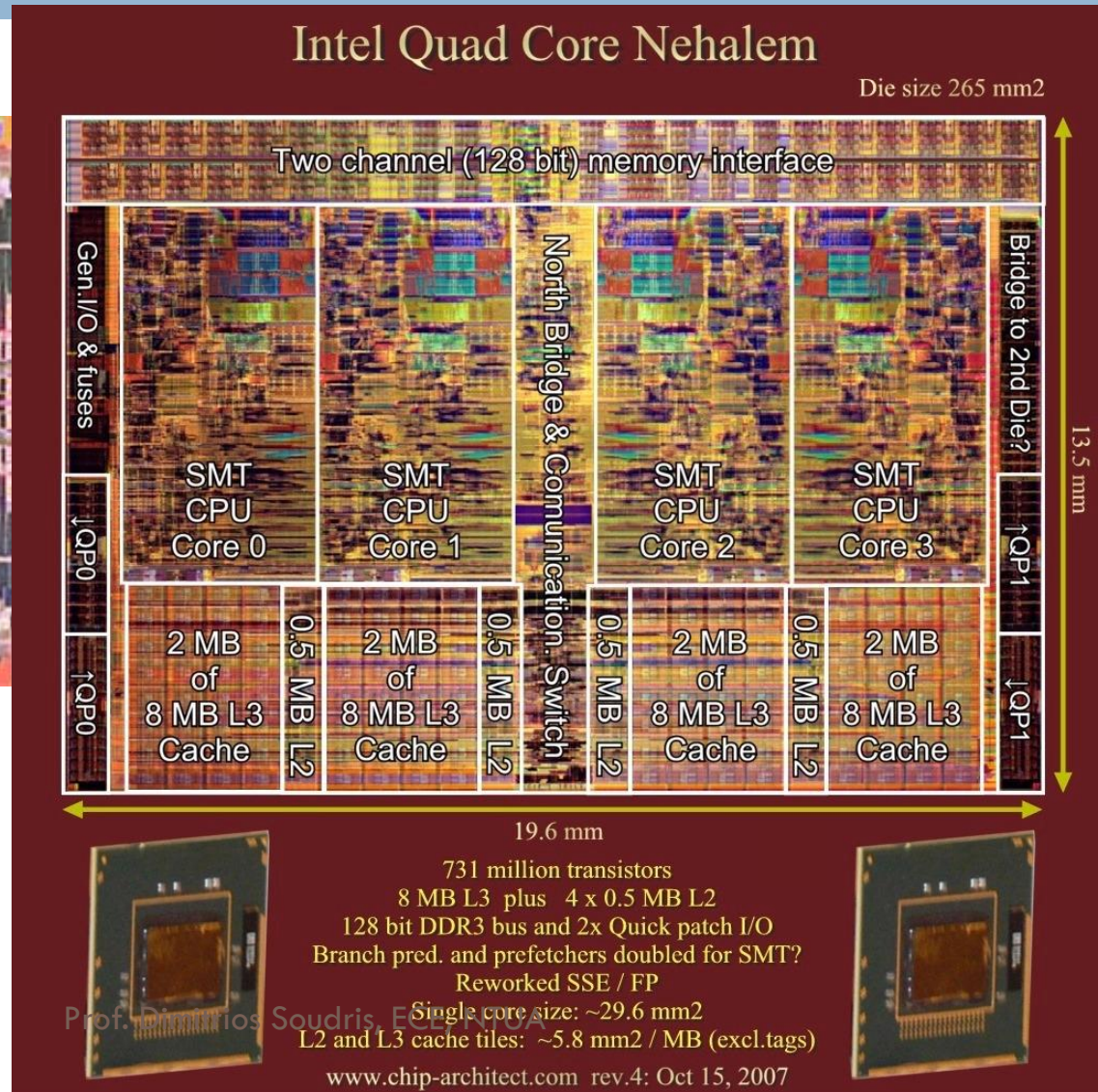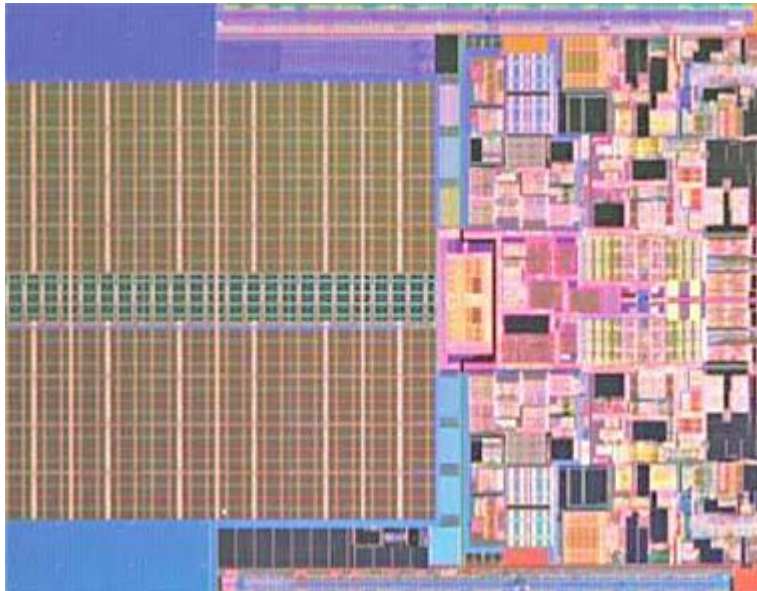
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Intel Microprocessor – Pentium III

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Intel Duo and Quad

Intel Quad Core Nehalem
Die size 265 mm2

Two channel (128 bit) memory interface

Gen.I/O & fuses

SMT CPU Core 0

SMT CPU Core 1

North Bridge & Comunication. Switch

SMT CPU Core 2

SMT CPU Core 3

Bridge to 2nd Die?

13.5 mm

↑QP0

↓QP0

2 MB of 8 MB L3 Cache

0.5 MB L2

2 MB of 8 MB L3 Cache

0.5 MB L2

0.5 MB L2

2 MB of 8 MB L3 Cache

0.5 MB L2

2 MB of 8 MB L3 Cache

↑QP1

↓QP1

19.6 mm

731 million transistors
8 MB L3 plus   4 x 0.5 MB L2
128 bit DDR3 bus and 2x Quick patch I/O
Branch pred. and prefetchers doubled for SMT?
Reworked SSE / FP
Single core size: ~29.6 mm2
L2 and L3 cache tiles: ~5.8 mm2 / MB (excl.tags)

www.chip-architect.com rev.4: Oct 15, 2007

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INTEL i7 core

ARM Επεξεργαστής

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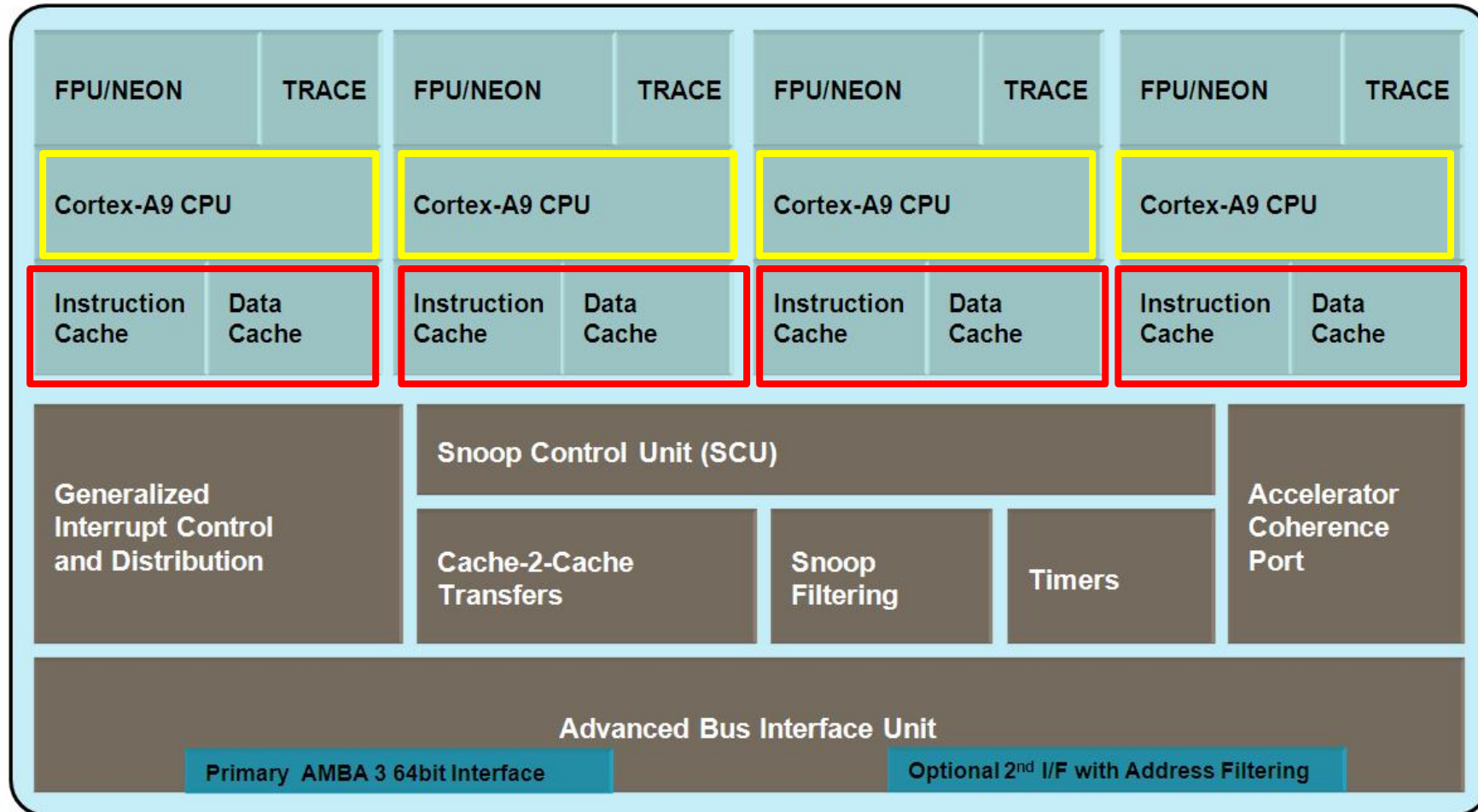
Επεξεργαστής Cell για Playstation3

Cell Broadband Engine Processor
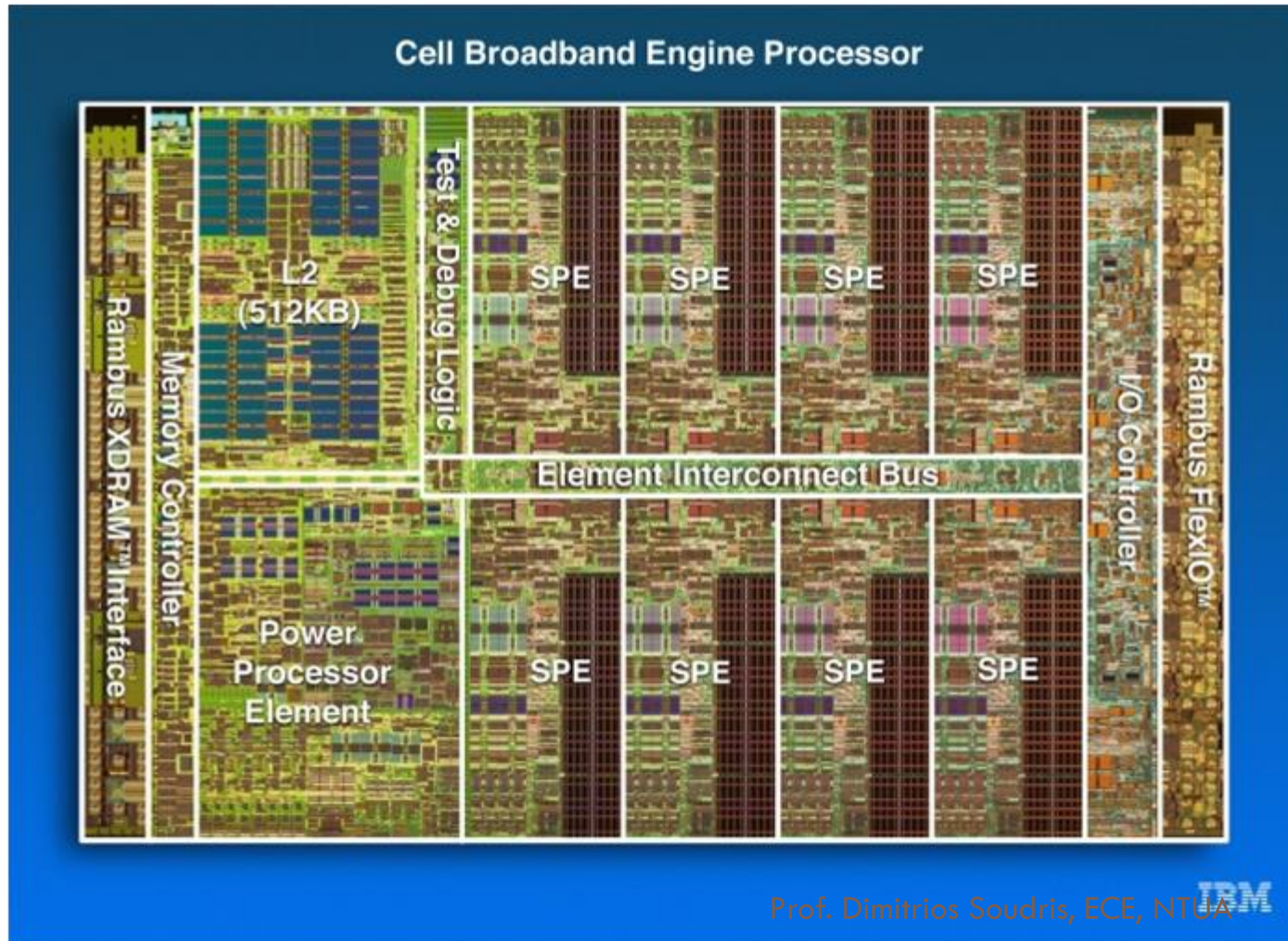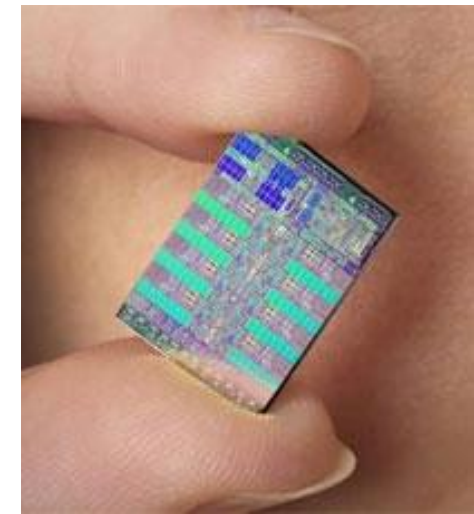
Transistor cost
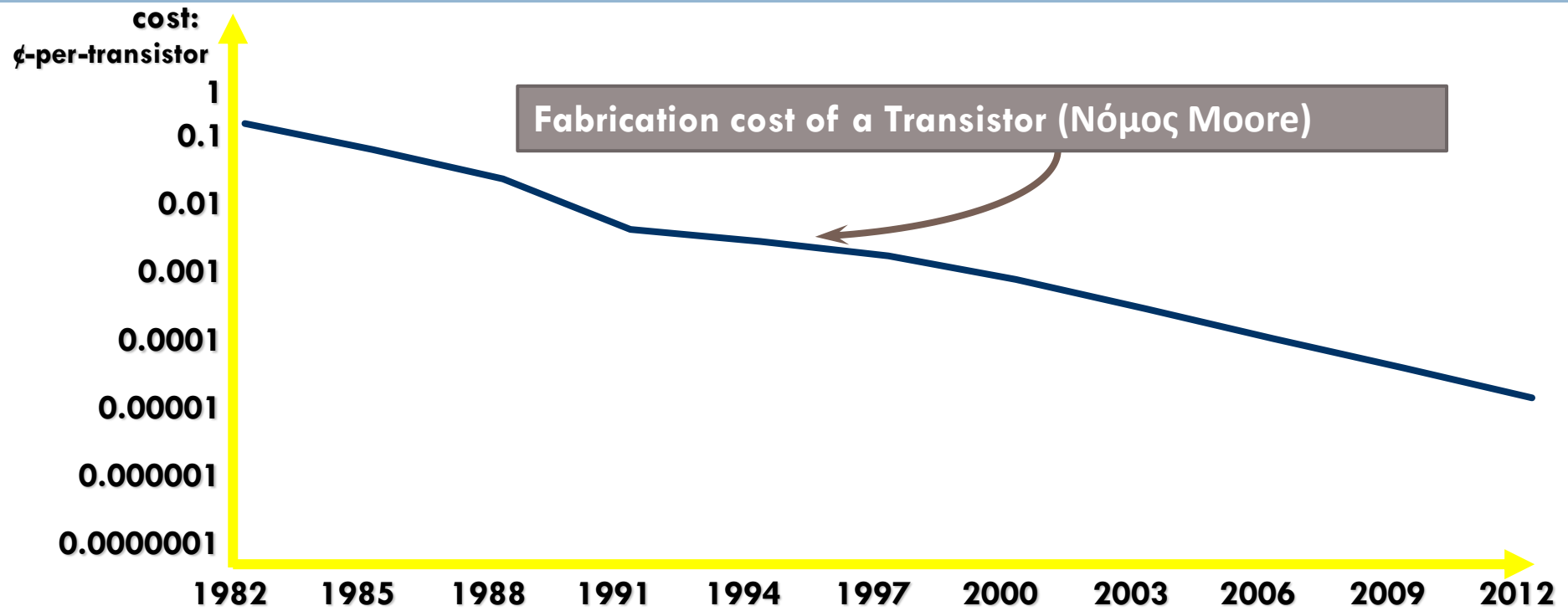
Design criteria of Digital Integrated Circuits

- **Performance (or speed)**

- **Silicon Area**

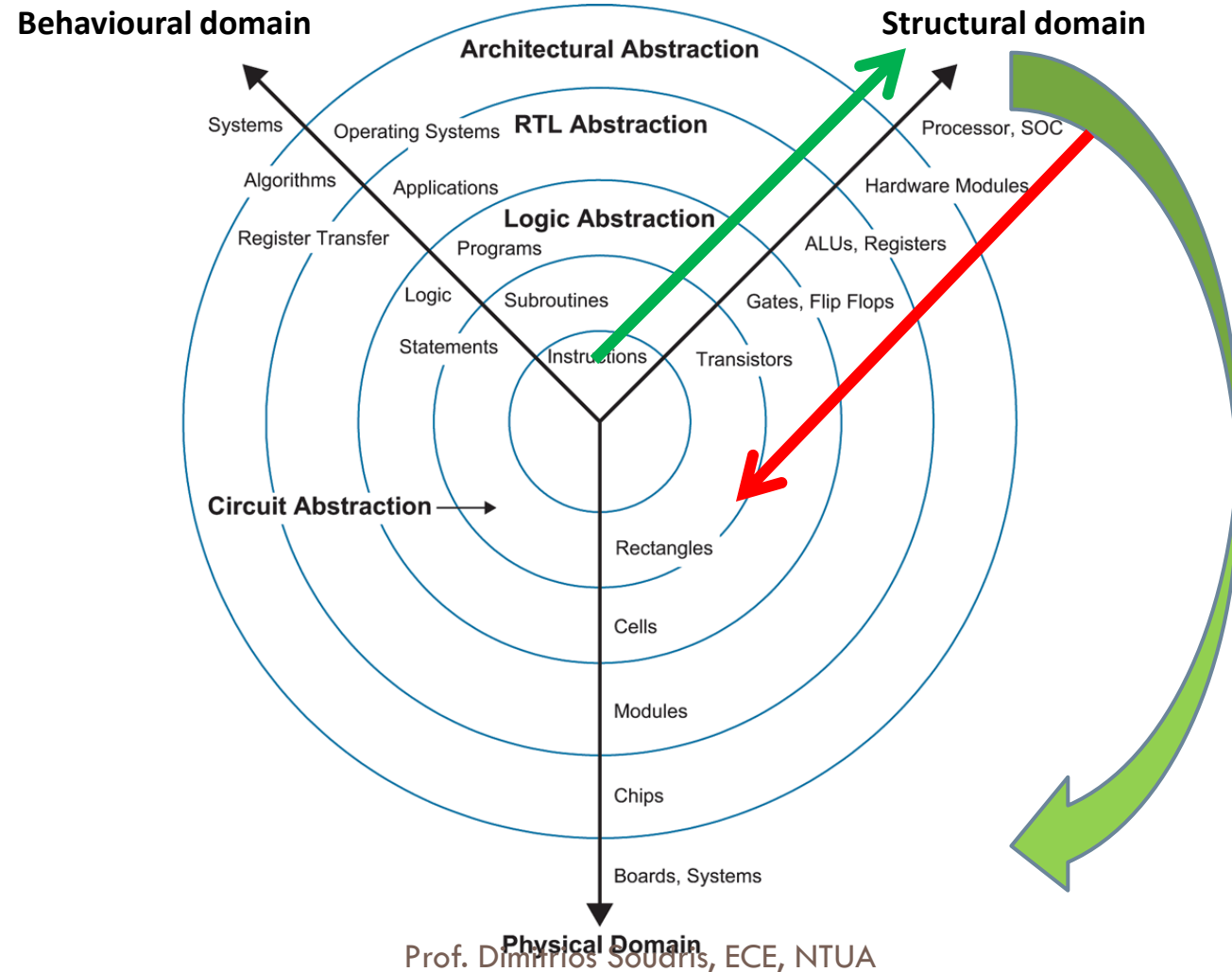- **Power consumption**

- **Temperature - Heat Dissipation**

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Memory = Performance Bottleneck

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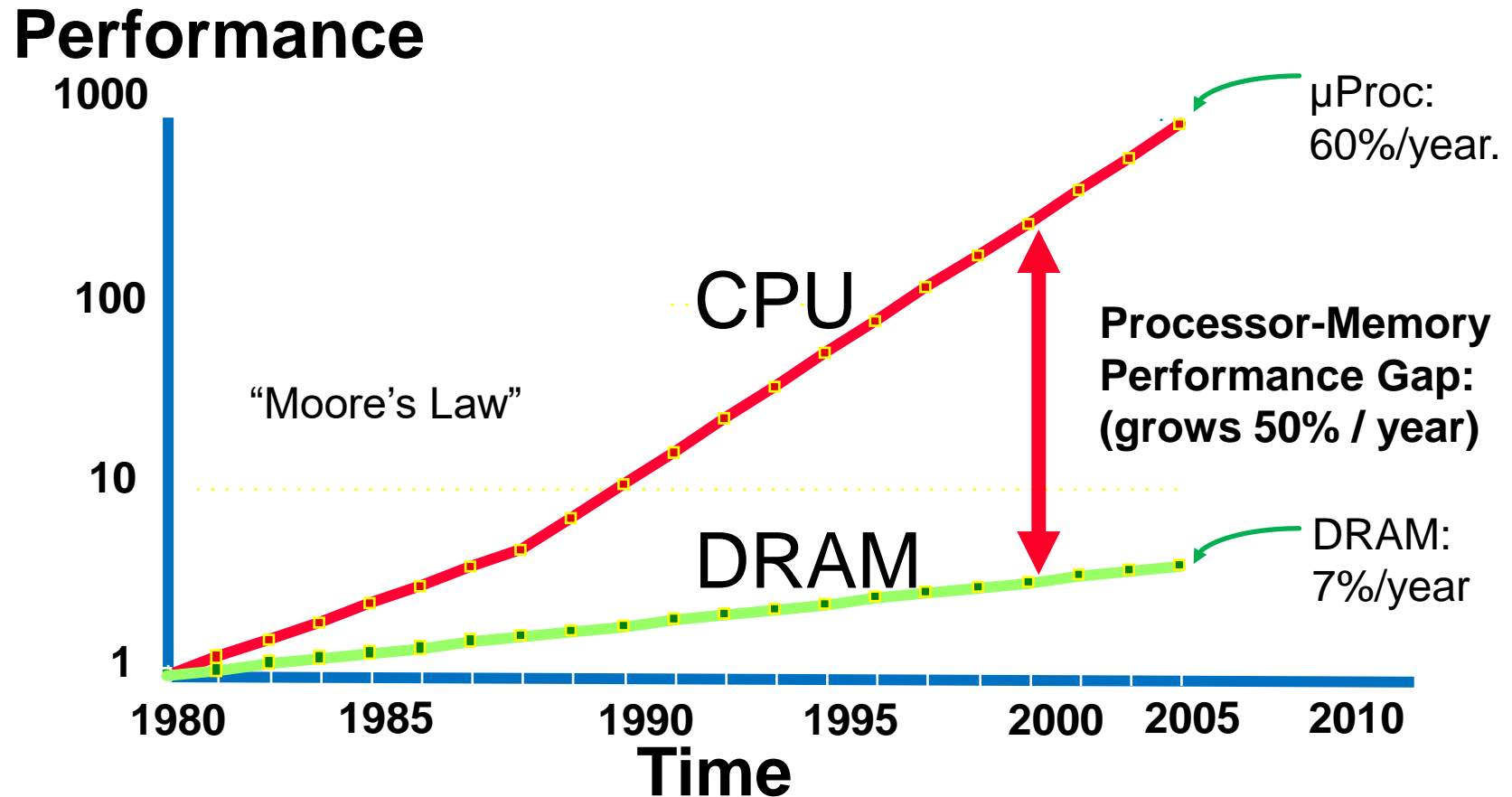
Y-Chart – Domains & Design Levels

Behavioural domain

Structural domain

Architectural Abstraction

RTL Abstraction

Systems

Operating Systems

Processor, SOC

Algorithms

Applications

Hardware Modules

Register Transfer

Logic Abstraction

ALUs, Registers

Programs

Logic

Subroutines

Gates, Flip Flops

Statements

Instructions

Transistors

Circuit Abstraction →

Rectangles

Cells

Modules

Chips

Boards, Systems

Physical Domain

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FIG 8.1 Gajski-Kuhn Y chart